WHAT IS CLAIMED IS:

1. A semiconductor structure having electrostatic discharge (ESD) protection, comprising:

an insulating layer;

a silicon layer on at least one side of the insulating layer;

a first transistor device formed in the silicon layer, the first transistor device having a source region and a drain region; and

a second transistor device formed in the silicon layer, the second transistor device having a source region and a drain region;

wherein

the first transistor device and the second transistor device are connected in series such that the drain region of the first transistor device and the source region of the second transistor device are in a shared region of the silicon layer;

the shared region has a depth that does not extend through the silicon layer to the insulating layer; and

the first and second transistor devices form a single parasitic bipolar device in the silicon layer such that the first and second transistor devices exhibit simultaneous snapback during an ESD event.

2. The structure of claim 1, wherein both the first and second transistor devices are either NMOS transistors or PMOS transistors.

3. The structure of claim 1, wherein the insulating layer comprises a buried oxide layer.

4. The structure of claim 1, wherein the silicon layer has a thickness in a range between about 10 nm and about 100 nm.

5. The structure of claim 4, wherein the shared region has a thickness in a range between about 5% and about 80 % of the thickness of the silicon layer.

6. The structure of claim 1, wherein the shared region has a thickness in a range between about 0.5 nm and about 80 nm.

7. The structure of claim 1, wherein both the first and second transistor devices are NMOS transistors each having a polysilicon gate structure above a p-type doped body in the silicon layer and the shared region is an n-type doped region in the silicon layer between the polysilicon gate structures of the NMOS transistors.

8. The structure of claim 7, further comprising a silicide layer on one or more of the n-type doped regions not including the shared region.

9. The structure of claim 1, wherein both the first and second transistor devices are PMOS transistors each having a polysilicon gate structure above a n-type doped body in the silicon layer and the shared region is a p-type doped region in the silicon layer between the polysilicon gate structures of the PMOS transistors.

10. The structure of claim 9, further comprising a silicide layer on one or more of the p-type doped regions not including the shared region.

11. A process of forming a semiconductor structure having electrostatic discharge (ESD) protection, comprising:

forming a first gate structure and a second gate structure on a first region of a silicon layer on a silicon-on-insulator (SOI) wafer, the first region having a first dopant, the SOI wafer having an insulating layer at a depth below an outer surface of the silicon layer;

in a first doping step, doping with a second dopant a source region for the first gate structure, a drain region for the second gate structure and a shared region between the first gate structure and the second gate structure such that the second dopant does not extend through the silicon layer to the depth of the insulating layer in the shared region;

in a second doping step, doping with a third dopant the drain region and the source region so that the third dopant extends through the silicon layer to the depth of the insulating layer.

12. The process of claim 11, wherein the shared region functions both as a drain for the first gate structure and a source for the second gate structure.

13. The process of claim 11, wherein the insulating layer comprises a buried oxide layer.

14. The process of claim 11, further comprising applying a silicide to the surface of the source region and the drain region.

15. The process of claim 11, wherein the first doping step includes ion implantation of the second dopant type having a dosage within a range between about 1 x 10^{12} atoms per cm^2 and about 1 x 10^{14} atoms per cm^2, and implantation energies in a range between about 10 KeV and about 100 KeV.

16. The process of claim 11, wherein the second doping step includes ion implantation of the second dopant type having a dosage within a range between about 1 x 10^{14} atoms per cm^2 and about 1 x 10^{16} atoms per cm^2, and implantation energies in a range between about 30 KeV and about 200 KeV.

17. The process of claim 11, further including a thermal budget having a temperature range of between about 900 C and about 1100 C and an anneal time range of between about 2 minutes and about 4 hours.

18. The process of claim 11, wherein the first doping step is a lightly doped drain (LDD) process.

19. The process of claim 11, wherein the source region, the drain region and the silicon layer under the shared region form a single parasitic bipolar transistor.

20. A process of forming a semiconductor structure having electrostatic discharge (ESD) protection, comprising:

in a first doping step, doping with a first dopant a first region of a silicon layer on a silicon-on-insulator (SOI) wafer, the SOI wafer having an insulating layer at a depth below an outer surface of the silicon layer;

forming a first gate structure and a second gate structure on the first region of the silicon layer;

in a second doping step, doping with a second dopant a source region for the first gate structure, a drain region for the second gate structure and a shared region between the first gate structure and the second gate structure such that the second dopant does not extend through the silicon layer to the depth of the insulating layer in the shared region;

in a third doping step, doping with a third dopant the drain region and the source region so that the third dopant extends through the silicon layer to the depth of the insulating layer.